Nonvolatile memory with switching interfacial polar structures of nano Si-in-mesoporous silica

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We show an artificially engineered electret with Si nanocrystals embedded in mesoporous silica for nonvolatile memory. We attribute the polarization to from polar layers lying at the interfaces between one-side bonded Si nanocrystals and mesoporous silica matrix. Under external field, the Si nanocrystals could be displaced in the porechannels causing displaced charge distributions and therefore a field-controllable electric polarization. Nonvolatile memory is demonstrated with a metal-oxide-semiconductor field-effect transistor. © *2009 American Institute of Physics*.
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To satisfy the ever-increasing need for information flow and storage, the industry of semiconductor integrated circuits (ICs) has eagerly hunted for an ideal semiconductor memory technology with the high speed of static random access memory (RAM), the nonvolatility of flash, and the density of dynamic RAM.[1] Nonvolatile memories (NVMs) can retain the data even when power is interrupted and are becoming a crucial component for the society of efficient energy utilization. In this regard, NVM based on the concept of storing information into the states of electric polarization had attracted much interest. In a ferroelectric field effect transistor with the gate dielectric layer being replaced by a ferroelectric thin film,[2–4] the electric polarization of the gate can be sensed by monitoring the magnitude of the source-drain current,[2–4] offering high speed random access,[5] low power consumption,[2,4,5] and nonvolatility.[1]

The spontaneous polarization of a ferroelectric crystal with a noncentrosymmetric structure is mainly due to permanent dipoles that can switch directions under an action of electric field.[6] Bulk silicon does not possess ferroelectric properties due to the diamond structure with centrosymmetry. To realize ferroelectric RAMs (FeRAM), tremendous efforts have been made to integrate nonsilicon-based ferroelectric films, such as lead zirconate titanate (PZT) and strontium bismuth tantalite (SBT),[2,6] with the mature silicon memory technology. However, the interface reactions between PZT (SBT) and the Si substrate often generate mobile ions and lead to low data retention time.[2,3,7]

Recently, we had shown that interfacial properties could be employed to yield multifunctionality[8] with polar Si–O nanostructures formed by asymmetrically embedding Si nanocrystals (nc-Si) in mesoporous silica (MS). In this letter, a full silicon-based metal-oxide-semiconductor field-effect transistor (MOSFET) NVM was demonstrated by using the artificially engineered electret.[9] Figure 1(a) presents the schematic of the NVM cell, where the electret film is sandwiched between two oxide buffer layers to serve as the gate dielectrics.

We prepared the test samples of nc-Si/MS by first depositing a 10-nm-thick SiO_2 buffer layer and then spin coating a 90-nm-thick MS nanotemplate layer on *n*- or *p*-type silicon. We thereafter synthesized Si nanocrystals in the MS templates with the high-density inductively coupled plasma method.[8] By invoking an enhancement effect with an electrically biased substrate similar to the gap-filling/etching process used in IC manufacturing, we can create one-side bonded silicon nanocrystals with polar layer structures at the interfaces of nc-Si and MS as illustrated in Fig. 1(a). The biased growth condition can be prepared by applying an electrical power of 300 W at 300 kHz on the substrate during the synthesis of Si nanocrystals. Finally a 10-nm-thick SiO_2

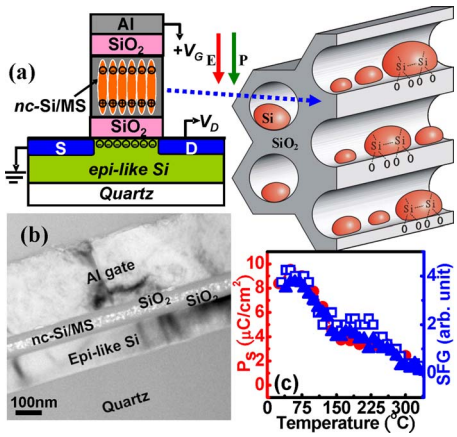

FIG. 1. (Color online) (a) Schematic diagram showing the one-side bonding geometry of Si nanocrystals in porechannels (right plot). A field-effect transistor structure with an $Al/SiO_2/nc\text{-}Si\text{-}in\text{-}MS/SiO_2$ gate stack on an epilike Si layer was depicted in the left plot of (a) and its cross-sectional TEM image in (b). (c) The SFG signal is presented as the film temperature is increased (open squares) or decreased (filled triangles). For comparison, the temperature dependence of electric polarization is shown with filled circles.

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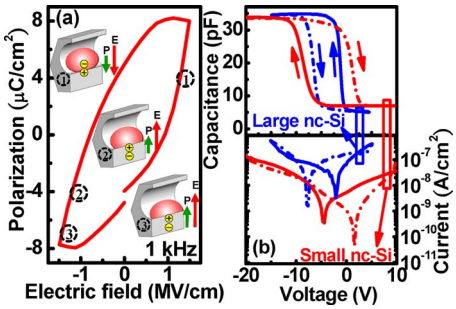

FIG. 2. (Color online) (a) The *P-E* hysteresis characteristics of the 90-nm-thick Si–O polar layers sandwiched with 10-nm-thick SiO_2 buffer layers in a MIM structure. Schematic drawings are presented in the inset to illustrate the switching process. The centers of gravity of the positive and negative charge distributions are labeled by ⊕ and Θ, respectively. (b) *C-V* hysteresis (top) and *I-V* characteristic curves (bottom) of a MOS capacitor containing an oxide stack identical to that in (a). For comparison, the *C-V* hysteresis of a MOS capacitor containing larger nc-Si contacting with the porechannels of MS (solid and dashed curves in blue) is also presented. Solid and dashed curves indicate the characteristics with a voltage sweep from positive to negative and from negative to positive, respectively. The top electrode pad of the device was made of aluminum film and 400-μm in diameter.

layer was deposited on the MS films and an electrode was then formed to complete MOS and metal-insulator-metal (MIM) structures for capacitance-voltage (*C-V*) and polarization-electric field (*P-E*) measurements, respectively.

Optical sum-frequency generation (SFG) is sensitive to surface and polar structure of a material[8,10] and hereby was applied to verify the existence of the polar bonding layers in nc-Si/MS. The generated SFG signal[8] is presented in Fig. 1(c) as the open squares when the film temperature was raised from room temperature to 350 °C. Above this temperature, the SFG signal disappears. The curve with filled triangles displays the SFG signal as the film temperature was decreased from 350 °C to room temperature. The two curves are similar to each other, revealing the highly reversible nature of the SFG susceptibility.[11]

To verify that a nonvanishing electric polarization can be yielded from the polar bonding structure in nc-Si/MS with direction switchable with an external electric field, we probed the electrical polarization in the insulation layer of SiO_2 (10 nm)/nc-Si-in-MS (90 nm)/SiO_2 (10 nm) with *P-E* measurements.[11] The results are presented in Fig. 2(a). The polarization of the sample at $E=0$ V was found to be 5 $\mu C/cm^2$, which is much larger than the reported values for iron-passivated porous silicon.[12] The temperature dependence of saturated polarization P_s from the *P-E* measurements is presented in Fig. 1(c) with filled circles. Striking similarity between the temperature-dependent behaviors of electric polarization and SFG was observed, suggesting the SFG susceptibility and the electric polarization of the one-side bonded nc-Si-in-MS to have the same origin. Under the dipole approximation, SFG is necessarily allowed on surface/at an interface or in a film with polar structure. We therefore attribute the results shown in Figs. 1(c) and 2(a) to originate from the polar structure existing in the artificially engineered electret.

Typical *C-V* characteristics of a MOS structure with a similar oxide stack of SiO_2/nc-Si-in-MS/SiO_2 on a *p*-type silicon substrate are presented in Fig. 2(b). A clockwise hysteresis loop with a positive-to-negative-to-positive voltage sweep was observed [see the red-colored curve in Fig. 2(b)],[4,7] yielding a memory window of 10 V. We had also verified that the *C-V* hysteresis loop changes from clockwise for samples prepared on *p*-type silicon to counterclockwise on *n*-type silicon substrate.[2,4,7] Note that charging (discharging) of quantum dots (QDs) by electrons (holes) via a tunneling process can shift the flatband voltage to a more (less) positive value.[13] This leads to a counterclockwise[14] hysteresis loop on *p*-type silicon when a positive-to-negative-to-positive voltage sweep is carried out, which contradicts with what we had observed. Although a clockwise *C-V* hysteresis loop can also be yielded with charged QDs, the clockwise *C-V* hysteresis can only be generated as the sweep range of applied voltage is sufficiently large to enable the charged QDs to be neutralized by injected carriers.[15] We found that our clockwise *C-V* hysteresis loop on *p*-type silicon substrates is essentially independent of the sweep range. Furthermore, the leakage current through the SiO_2/nc-Si-in-MS/SiO_2 stack is below 1×10^{-7} A/cm^2 in the entire sweep range [see Fig. 2(b)], suggesting that the charging/discharging effect via a tunneling process in our sample is fairly minor.[15]

The polar nature of the one-side bonded nc-Si/MS MOS capacitor is expected to disappear as the Si nanodots grow up to sufficiently large, making the circumferences of each Si nanodots to touch on the wall of the pore channels. In this case, we observed a counterclockwise *C-V* hysteresis, revealing the charge localization effect as shown by the blue-colored curves in Fig. 2(b). Assuming both of the *C-V* characteristics of nc-Si/MS capacitors to be produced completely by charge localization, we are expecting to find that a nc-Si/MS layer with larger nc-Si shall result in an increased gate current [see Fig. 2(b)], and therefore a wider memory window[16] (due to a higher charge density in the QDs). However, as shown in Fig. 2(b), an opposite result was observed. By summarizing these discoveries, we therefore attribute the clockwise *C-V* hysteresis of the MOS capacitor with one-side bonded nc-Si/MS on *p*-type silicon to originate from electric dipole layers.[17] In this case, the built-in dipole field from an electrical polarization in the MOS capacitor would either enhance or screen the external field depending on the direction of the applied field.

The quasipermanent interfacial polarization in our one-side bonded nc-Si/MS is switchable with an external field [Fig. 2(a)]. This is understandable by noting that the Si nanocrystals in porechannels can displace under an action of electric field, causing a displacement of the center of gravity of the negative charge distribution [labeled by Θ in the inset of Fig. 2(a)] relative to that of the positive charge distribution (labeled by ⊕ in the inset of Fig. 2(a)). We calculated that a relative displacement of the charge distributions across the interfacial layers of nc-Si/MS, which have a thickness of about 3–4 Å, can readily produce an electric polarization as large as 5 $\mu C/cm^2$.[8] Schematic drawings are presented in the inset of Fig. 2(a) to facilitate the illustration of the switching process.

To test the feasibility of nc-Si/MS as a NVM, a MOSFET with a 55-nm-thick nc-Si/MS electret layer was fabricated. A 20-nm-thick oxide buffer layer underneath and above the nc-Si/MS film was introduced to inhibit charge transportation through the gate structure. The MOSFET with a channel length of 6 μm and a channel width of 25 μm was fabricated with a 120-nm-thick epilike silicon layer[18] on quartz substrate. Figure 1(b) shows the cross-sectional trans-

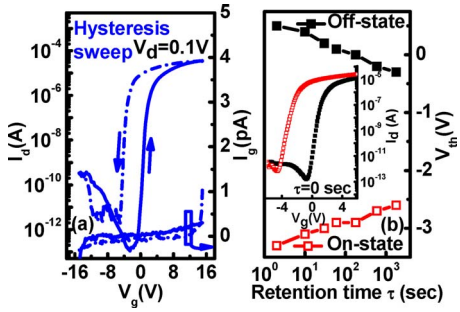

FIG. 3. (Color online) (a) A hysteretic switching I_d-V_g curve for a MOSFET device with a gate structure of Al/SiO_2/nc-Si-in-MS/SiO_2 with a fairly low gate current I_g was shown. (b) Data retention of the MOSFET is shown as the decaying behavior of threshold voltages $V_{th,on}$ (open squares) and $V_{th,off}$ (filled squares) with time (τ) in the on state and off state. The inset shows that the transfer characteristics of the MOSFET at $\tau=0$ after the MOSFET was programmed to the on and off state with 20 ms duration V_g pulse of 15 and −15 V, respectively.

mission electron microscopy (TEM) image of the device around the gate region. The drain currents I_d as a function of gate voltage V_g are presented in Fig. 3(a). By keeping the drain voltage V_d at 0.1 V while increasing V_g from −15 to +15 with an increment of 0.1 V, we can switch the device from the "off" state to the "on" state with an off-state threshold voltage $V_{th,off}=0.7$ V. On the contrary, as the V_g sweeps from +15 to −15, the device can be switched off with an on-state threshold voltage $V_{th,on}=-4.3$ V and yields a memory window of $\Delta V=V_{th,off}-V_{th,on}=5$ V.[3,7] The memory window saturates at 5 V as long as maximum sweeping voltage $|V_g|$ is greater than 12 V. The drain current I_d of the MOSFET in the off state is about 1×10^{-12} A with $V_g=0$ V. In the on state, I_d can reach the level of 1×10^{-5} A with $V_g=0$ V. Thus, a contrast ratio of the on to the off state larger than 7 orders of magnitude is achieved [see the inset of Fig. 3(b)].

Note that the major causes of the short data retention time in a typical FeRAM can be (1) depolarization field effect and (2) finite gate leakage current.[3,5] Since our nc-Si/MS is intrinsically a low permittivity material, the depolarization field shall not cause a problem. The data retention time in a FeRAM device with a remnant polarization P_r, gate leakage current density I, and a trapping probability of α can be estimated with $\tau=P_r/I\alpha$.[5] In our MOSFET with nc-Si/MS electret, the measured remnant polarization $P_r=5$ $\mu C/cm^2$ and gate leakage current density 3×10^{-7} A/cm^2 implies a data retention time of $T=10^5$ s to be achievable. The estimated retention time[5] with $I_g\sim0.5$ pA, the gate area and a trapping probability of 10^{-4} agrees well with the measured result shown in Fig. 3(b), where the variation of threshold voltages $V_{th,on}$ (open squares) and $V_{th,off}$ (filled squares) as a function of lasting time in the on state and off state is presented.

In conclusion, we report an artificially engineered NVM electret material synthesized by embedding nc-Si in mesoporous silica. Material characterizations indicated that the nanocrystals form noncentrosymmetric bonding with the host silica matrix, yielding highly stable interfacial polar structures. We fabricated a MOSFET by using a nc-Si/MS layer in place of the gate dielectrics. The device exhibits a polarization-induced memory window of 5 V, a very low gate leakage and high ratio of the on state to the off state, promising for a fully silicon-based NVM technology with the potential of low cost and scalable to nanometer dimensions.

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